Amendment to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listings of Claims

Claims 1-11 (canceled)

Claim 12 (new): An electrostatic-breakdown-preventive and protective circuit for a semiconductor-device, the circuit comprising:

a first power-source line and a first ground line for supplying bias to a first internal block;

a second power-source line and a second ground line for supplying bias to a second internal block;

a third power-source line and a third ground line for supplying bias to an input/output circuit portion;

at least one of a first protective transistor provided between the first power-source line and the second power-source line and a second protective transistor provided between the first ground line and the second ground line;

a third protective transistor disposed between the third power-source line and the third ground line; and

a connection line for transferring an output signal of the first internal block as an input signal of the second internal block,

wherein at least one of the first protective transistor and the second protective transistors is disposed in a vicinity of the connection line.

Claim 13 (new): The electrostatic-breakdown-preventive and protective circuit according to claim 12, wherein the first, second and third ground lines are connected to a ground pad, and the second protective transistor is provided between the first ground line and the second ground line.

Claim 14 (new): The electrostatic-breakdown-preventive and protective circuit according to claim 13, wherein the first and second power-source lines are respectively connected to power-source pads, and the power-source pads supplying differential potential level to the first and second power-source lines.

Claim 15 (new): The electrostatic-breakdown-preventive and protective circuit according to claim 12, wherein the semiconductor-device having the electrostatic-breakdown-preventive and protective circuit is formed on a SOI substrate.

Claim 16 (new): The electrostatic-breakdown-preventive and protective circuit according to claim 12, wherein each of the first protective transistor and the second protective transistor, a compound layer of silicon and metal is formed on the entirety of a surface between a contact hole for connecting an impurity diffusion layer serving as a source and a drain with a metallic wiring, and a gate.

Claim 17 (new): The electrostatic-breakdown-preventive and protective circuit according to claim 16, wherein a distance in each of the first protective transistor and the second protective transistor from the contact hole for connecting the impurity diffusion layer serving as the source and the drain of the protective transistor with the metallic wiring, to the gate of the protective transistor has a minimum value possible in a fabrication process.

Claim 18 (new): The electrostatic-breakdown-preventive and protective circuit for a semiconductor-device, the circuit comprising:

a first power-source line and a first ground line for supplying bias to a first internal block;

a second power-source line and a second ground line for supplying bias to a second internal block;

a third power-source line and a third ground line for supplying bias to an input/output circuit portion;

a protective transistor disposed between the third power-source line and the third ground line;

a connection line for transferring an output signal of the first internal block as an input signal of the second internal block; and

at least one of a first resistor one end of which is connected to the first power-source line and another end of which is connected to the second power-source line, and a second resistor one end of which is connected to the first ground line and another end of which is connected to the second ground line,

wherein at least one of the first resistor and the second resistor is disposed in a vicinity of the connection line.

Claim 19 (new): The electrostatic-breakdown-preventive and protective circuit according to claim 18, wherein the first, second and third ground lines are connected to a ground pad, and the second resistor is provided between the first ground line and the second ground line.

Claim 20 (new): The electrostatic-breakdown-preventive and protective circuit according to claim 19, wherein the first and second-power source lines are respectively connected to power-source pads, and the power-source pads supplying differential potential level to the first and second power-source lines respectively.

Claim 21 (new): The electrostatic-breakdown-preventive and protective circuit according to claim 18, wherein the semiconductor-device having the electrostatic-breakdown-preventive and protective circuit is formed on a SOI substrate.

Claim 22 (new): An electrostatic-breakdown-preventive and protective circuit for a semiconductor-device, the circuit breakdown comprising:

a first power-source line and a first ground line for supplying bias to a first internal block;

a second power-source line and a second ground line for supplying bias to a second internal block;

a third power-source line and a third ground line for supplying bias to an input/output circuit portion;

at least one of a first protective element provided between the first power-source line and the second power-source line and a second protective element provided between the first ground line and the second ground line;

a third protective element disposed between the third power-source line and the third ground line;

a connection line for transferring an output signal of the first internal block as an input signal of the second internal block,

wherein at least one of the first protective element and the second protective element is disposed in a vicinity of the connection line.

Claim 23 (new): The electrostatic-breakdown-preventive and protective circuit according to claim 22, wherein the first, second and third ground lines are connected to a ground pad, and the second protective element is provided between the first ground line and the second ground line.

Claim 24 (new): The electrostatic-breakdown-preventive and protective circuit according to claim 23, wherein the first and second power-source lines are respectively connected to power-source pads, the power-source pads supplying differential potential level to the first and second power-source lines respectively.

Claim 25 (new): The electrostatic-breakdown-preventive and protective circuit according to claim 22, wherein the semiconductor-device having the electrostatic-breakdown-preventive and protective circuit is formed on a SOI substrate.

Claim 26 (new): The electrostatic-breakdown-preventive and protective circuit according to claim 22, wherein the first, second and third protective elements are first, second and third protective transistors.

Claim 27 (new): The electrostatic-breakdown-preventive and protective circuit according to claim 26, wherein at each of the first protective transistor and the second protective transistor, a compound layer of silicon and metal is formed on the entirety of a surface between a contact hole for connecting an impurity diffusion layer serving as a source and a drain with a metallic wiring, and a gate.

Claim 28 (new): The electrostatic-breakdown-preventive and protective circuit according to claim 27, wherein a distance in each of the first protective transistor and the second protective transistor form the contact hole for connecting the impurity diffusion layer serving as the source an the drain of the protective transistor with the metallic wiring, to the gate of the protective transistor has a minimum value possible in a fabrication process.

Claim 29 (new): The electrostatic-breakdown-preventive and protective circuit according to claim 22, wherein the first, second and third protective elements are resistors.